

**SUPERJUNCTION DEVICE AND  
PROCESS FOR ITS MANUFACTURE**

**ABSTRACT OF THE DISCLOSURE**

A process to make a low voltage (under 200 volts) superjunction device employs spaced P type implants into the generally central depth region of an epitaxially formed N layer. The wafer is then placed in a diffusion furnace and the spaced implants are driven upward and downward by 4 to 8 microns to form spaced P pylons in an N type epitaxial body. MOSgated structures are then formed atop each of the P pedestals. The total P charge of each pedestal is at least partially matched to the total N charge of the surrounding epitaxial material. The initial implant may be sandwiched between two discrete epitaxial layers.